



1FW  
\$

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Rajesh Tiwari, et al.

Docket No: TI-36211

Serial No: 10/663,948

Conf. No: 3857

Examiner: Phat X. Cao

Art Unit: 2814

Filed: 09/16/2003

For: DUAL DEPTH TRENCH TERMINATION METHOD FOR IMPROVING CU-BASED  
INTERCONNECT INTEGRITY

**ELECTION**

Commissioner For Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)**

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 11-24-04.

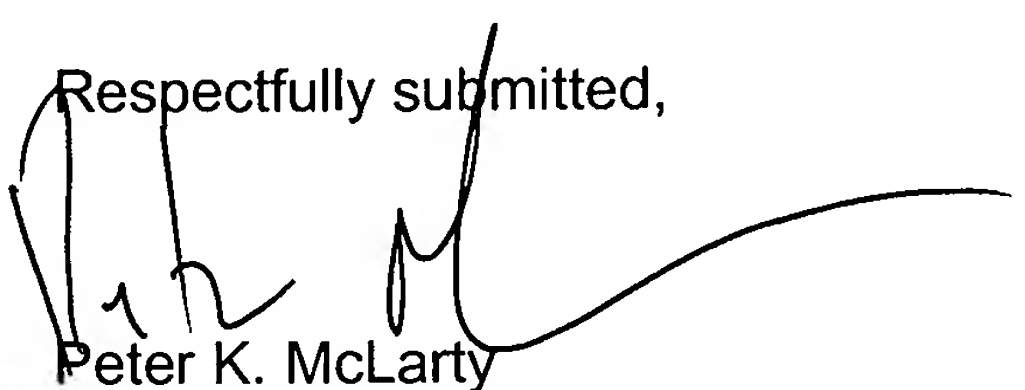
  
Ann Trent

Dear Sir:

This election is offered in response to the Examiner's restriction requirement mailed October 12, 2004.

Applicants hereby elect to pursue Group I of Claims 1-4 and 9, drawn to a process of making a semiconductor device, without traversing the Examiner's restriction requirement.

Respectfully submitted,

  
Peter K. McLarty  
Attorney for Applicants  
Reg. No. 44,923

Texas Instruments Incorporated  
P.O. Box 655474, MS 3999  
Dallas, TX 75265  
(972) 917-4258